In the claims:

Claim 1 (previously presented) A high-performance, high I/O ball grid array substrate, designed for integrated circuit flip-chip assembly and having two patterned metal layers, comprising:

an insulating layer having a first surface, a second surface and a plurality of vias filled with metal;

said first surface having one of said metal layers attached to provide electrical ground potential, and having a plurality of electrically insulated openings for outside electrical contacts;

an outermost insulating film protecting the exposed surface of said ground layer, said film having a plurality of openings filled with metal suitable for solder ball attachment;

said second surface having the other of said metal layers attached, portions thereof being configured as a plurality of electrical signal lines, further portions as a plurality of first electrical power lines, and further portions as a plurality of second electrical power lines, selected signal and power lines being in contact with said vias;

said signal lines being distributed relative to said first power lines such that the inductive coupling between them reaches at least a minimum value, providing high mutual inductances and minimized effective self-inductance;

said signal lines further being electromagnetically coupled to said ground metal such that cross-talk between signal lines is minimized; and

an outermost insulating film protecting the exposed surfaces of said signal and power lines, said film having a plurality of openings filled with metal suitable for contacting selected signal and power lines and chip solder bumps.

Claim 2 (previously presented) The substrate according to Claim 1 wherein the number of said I/O's ranges from about 100 to about 600.

Claim 3 (previously presented) The substrate according to Claim 1 wherein the thickness of said substrate is in the range from about 150 to 300 μm.

Claim 4 (previously presented) The substrate according to Claim 1 wherein said signal lines have a width between about 25 to 60 μm and are spaced to an adjacent line by insulating material of about 20 to 50 μm width.

Claim 5 (previously presented) The substrate according to Claim 1 wherein said first power lines have a width from about 200 to 500 μm.

Claim 6 (previously presented) The substrate according to Claim 1 wherein said signal lines are positioned in a proximity of about 20 to 50 μm to said first power lines, thus providing strong electromagnetic coupling, high mutual inductance and minimized effective self-inductance.

Claim 7 (previously presented) The substrate according to Claim 1 wherein said signal lines are positioned to provide strong electromagnetic coupling to power and ground lines and thus minimal coupling, or cross-talk, between said signal lines.

Claim 8 (previously presented) The substrate according to Claim 1 wherein said patterned metal layers are selected from a group consisting of copper, brass, aluminum, silver, or alloys thereof, and have a thickness in the range from about 7 to 15 μm.

Claim 9 (previously presented) The substrate according to Claim 1 wherein said insulating layer is made of organic material and is selected from a group consisting of polyimide, polymer strengthened by glass fibers, FR-4, FR-5, and BT resin;

said insulating layer having a thickness between about 70 and 150 μm.

Claim 10 (previously presented) The substrate according to Claim 1 wherein said vias are filled with copper, tungsten, or any other electrically conductive material.

Claim 11 (previously presented) The substrate according to Claim 1 wherein said second power lines are structured as distributed areas having wide geometries for minimizing self-inductance and merging into a central area supporting said chip.

Claim 12 (previously presented) The substrate according to Claim 1 wherein said outermost insulating films are glass-filled epoxies, polyimides, acrylics or other photo-imageable materials suitable as solder masks and have a thickness between about 50 and 100 μm.

Claim 13 (previously presented) The substrate according to Claim 1 wherein said openings for solder bump and solder ball attachments are made of copper including a flash of gold or palladium, or other wettable and solderable metals.

Claim 14 (previously presented) A high-performance, high I/O ball grid array package comprising:

a substrate having two patterned metal layers, comprising:

an insulating layer having a first surface, a second surface and a plurality of vias filled with metal;

said first surface having one of said metal layers attached to provide electrical ground potential, and having a plurality of electrically insulated openings for outside electrical contacts;

an outermost insulating film protecting the exposed surface of said ground layer, said film having a plurality of openings filled with metal suitable for solder ball attachment;

said second surface having the other of said metal layers attached, portions thereof being configured as a plurality of electrical signal lines, further portions as a plurality of first electrical power lines, and further portions as a plurality of second electrical power lines, selected signal and power lines being in contact with said vias;

said signal lines being distributed relative to said first power lines such that the inductive coupling between them reaches at least a minimum value, providing high mutual inductances and minimized effective self-inductance;

said signal lines further being electromagnetically coupled to said ground metal such that cross-talk between signal lines is minimized; and

an outermost insulating film protecting the exposed surfaces of said signal and power lines, said film having a plurality of openings filled with metal suitable for contacting selected signal and ground lines and chip solder bumps;

an integrated circuit chip having an active surface including solder bumps, said solder bumps adhered to said plurality of openings in said outermost insulating film protecting said signal and power lines; and

solder balls attached to said plurality of openings in said outermost insulating film protecting said ground layer.

Claim 15 (previously presented) The package according to Claim 14 further comprising a polymeric encapsulant filling any gaps between said chip and said substrate, left void after said chip solder bumps are adhered to said plurality of openings in said outermost insulating film protecting said signal and power lines.

Claim 16 (previously presented) The package according to Claim 15 wherein said polymeric encapsulant is a polymeric precursor made of an epoxy base material filled with silica and anhydrides, requiring thermal energy for curing to form a polymeric encapsulant.

Claim 17 (previously presented) The package according to Claim 14 further comprising an encapsulation material surrounding said chip.

Claim 18 (previously presented) The package according to Claim 17 wherein said encapsulation material is a polymeric material selected from a group consisting of epoxy-based molding compounds suitable for adhesion to said chip, and fluoro-dielectric compounds supporting high-speed and high-frequency package performance.

Claim 19 (previously presented) The package according to Claim 17 further comprising an optional heat spreader positioned on the outer surface of said encapsulation material.

Claim 20 (previously presented) The package according to Claim 14 wherein said chip solder bumps comprise attach materials selected from a group consisting of tin, lead/tin alloys, indium, indium/tin alloys, solder paste, and conductive adhesive compounds.

Claim 21 (previously presented) The package according to Claim 14 wherein said solder balls comprise attach materials selected from a group consisting of tin/lead, tin/indium, tin/silver, tin/bismuth, solder paste, and conductive adhesive compounds.

Claim 22 (previously presented) The package according to Claim 14 wherein the thickness of said package is in the range from about 250 to 800 μm, excluding the thickness of the heat slug.

Claims 23 to 29 (canceled)

Claim 30 (previously presented) A packaged integrated circuit, comprising:

a substrate having first and second opposing surfaces, said substrate having:

a plurality of signal lines, a plurality of first power lines coupleable to a first power source, and a plurality of second power lines coupleable to a second power source, all on said second surface, at least one of said plurality of signal lines disposed between a pair of said plurality of first power lines, and said signal lines between said pair of said plurality of first power lines and said pair of said plurality of first power lines disposed between a pair of said second power lines; and

an integrated circuit chip mounted on said substrate.

Claim 31 (previously presented) The integrated circuit of Claim 30, wherein said signal lines are of a first width, said first power lines are of a second width different from said first, and said second power lines are of a third width different from said first and second widths.

Claim 32 (previously presented) The integrated circuit of Claim 31, wherein said third width is wider than said second width, and said second width is wider than said first width.

Claim 33 (previously presented) The integrated circuit of Claim 30, further comprising a ground plane on said first surface of said substrate.

Claim 34 (previously presented) A packaged integrated circuit, comprising:

a substrate having first and second opposing surfaces, said substrate having thereon:

a plurality of groups of lines, said plurality of groups of lines including groups of lines of at least three different widths disposed on said second surface of said substrate, said groups of lines arranged such that one or more lines in a first group of lines of a first width are disposed between lines of a second group of lines of a second width and lines in a said second group of lines of said second width are disposed between lines of said third width; and

an integrated circuit chip mounted on said substrate and coupled to at least some of said lines.

Claim 35 (previously presented) The integrated circuit of Claim 34, wherein said lines of said first width are signal lines, said lines of said second width are power lines coupled to a first voltage potential, and said lines of said third width are power lines coupled to a second voltage potential.

Claim 36 (previously presented) The integrated circuit of Claim 34, further comprising a ground plane on said first surface of said substrate.

Claim 37 (previously presented) A packaged integrated circuit, comprising:

a substrate having first and second opposing surfaces, said substrate having:

a plurality of signal lines, a plurality of first power lines coupled to a first power source, and a plurality of second power lines coupled to a second power source, all on said second surface, at least one of said plurality of signal lines disposed between a pair of said plurality of first power lines, and said signal lines between said pair of said plurality of first power lines and said pair of said plurality of first power lines disposed between a pair of said second power lines; and

an integrated circuit chip mounted on said substrate.

Claim 38 (previously presented) The integrated circuit of Claim 37, wherein said signal lines are of a first width, said first power lines are of a second width different from said first, and said second power lines are of a third width different from said first and second widths.

Claim 39 (previously presented) The integrated circuit of Claim 38, wherein said third width is wider than said second width, and said second width is wider than said first width.